DUELING DETECTORS

By James Janesick, Sarnoff Corp.

CMOS or CCD? The choice depends on the application.

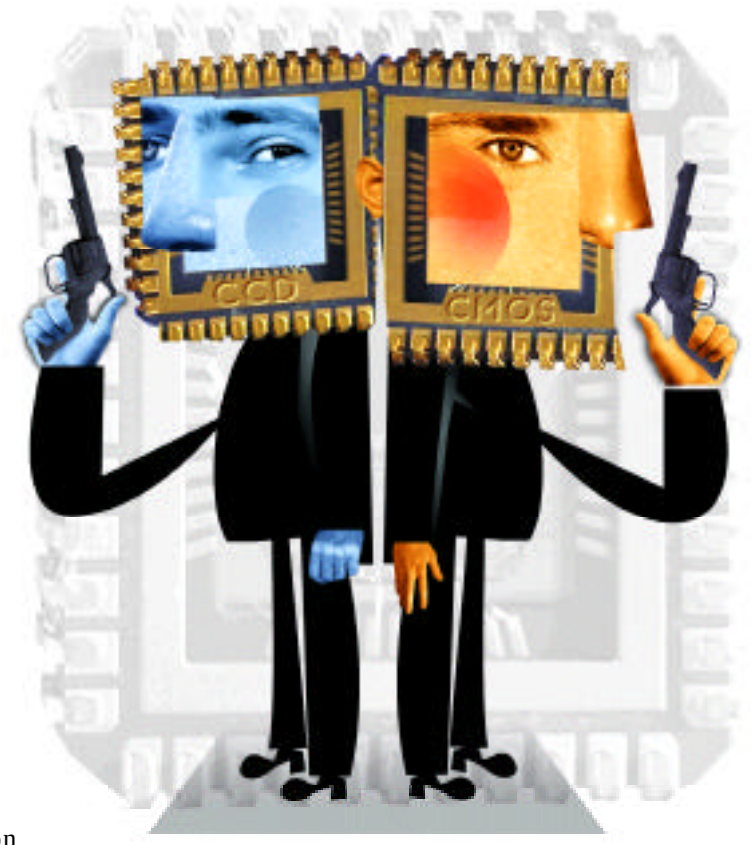

ILLUSTRATION BY WILLIAM RIESER

Nearly a decade has passed since complementary-metal-oxide-semiconductor (CMOS) imaging detectors began to make their move into the charge-coupled-device (CCD) detector arena. Initial claims made by proponents of the new technology generated intense competition between groups. This controversy has finally begun to subside, however, as clear indicators now show where performance strengths and weaknesses really lie. Contrary to some beliefs, both technologies will indeed coexist in the future.

This calm in the image community has come about through careful sensor characterization using absolute test methodologies.[1] The requirements of particular applications in terms of such variables as performance, level of integration, and cost, are becoming the primary drivers of CMOS and CCD selection. CMOS detectors are beginning to command the low-cost imaging market, for example, whereas CCDs are satisfying high-performance imaging needs (see ***oe****magazine*, January 2002, page 36).

The contrast in performance is most apparent when we consider scientific applications. We can make effective performance comparisons and future projections by reviewing the four operational tasks in generating an image: charge generation, charge collection, charge transfer, and charge measurement.

charge generation

The first operation, charge generation, is the ability of the sensor to intercept incoming photons and generate signal electrons through the photoelectric effect. This process is described by a performance parameter called quantum efficiency (QE). An ideal sensor would have 100% QE at all wavelengths, but nature is rarely this kind.

To achieve high response, sensor manufacturers must minimize three types of loss—absorption, reflection, and transmission. Absorption loss is associated with optically dead structures, which are typically located above and within the pixel. Reflection and transmission losses are inherent to the physical properties of silicon. At certain wavelengths, reflection loss is significant; for example, at 250 nm, reflection loss reaches 70%. Transmission loss takes place when incoming photons pass through the sensor's photosensitive volume, a region typically 10 μm-thick, without generating signal charge. This problem is pronounced at very long and very short wavelengths, i.e., the near-infrared (above 700 nm) and soft x-ray (below 0.2 nm) spectral regions.

CMOS arrays experience greater difficulty with absorption loss than CCDs because the metal-oxide-semiconductor

field-effect transistors (MOSFETs) incorporated in each pixel for readout are optically dead, and each pixel requires a minimum of three transistors (see figure 1). In that CCD pixels do not require active transistors for readout, they are constructed so that the entire pixel is sensitive, with a 100% fill factor (see figure 2). CMOS sensors also require several metal layers to interconnect MOSFETs. The busses are stacked and interleaved above the pixel, producing an "optical tunnel" through which incoming photons must pass. The metal stack is typically several microns high and can create a host of undesired optical effects for low f-number optical systems, including vignetting, pixel crosstalk, light scattering, and diffraction.

Using light shields above the pixel can control the problem, but it reduces the fill factor. The effect can also be somewhat counteracted by use of microlenses to help direct light into the pixel. Microlensed imagers, however, show a strong sensitivity dependence on incident photon wavelength and angle. In contrast, CCDs typically use thin (less than 0.4 μm) overlapping polysilicon gates to define the pixels, which lie close to the silicon surface. The CMOS issues above are mainly a concern for small pixel devices; for devices with pixels larger than 10 μm, QE performance for the two technologies are comparable.

To optimize QE performance, both types of imaging detectors can be thinned and illuminated from the rear side, delivering spectral response from the soft x-ray to the near-infrared spectral regions (from 0.1 to 1000 nm). Backside illumination eliminates absorption loss by producing a pixel with a 100% fill factor. Applying antireflection coatings eliminates reflection loss, leaving only transmission loss for the detector. Backside illumination has been used since the invention of the CCD and has yielded state-of-the-art detectors with QEs as high as 90% in the visible spectrum.

Because incident light in back-thinned devices impinges on the back side rather than the front side of the pixel, thinning could potentially circumvent the CMOS optical-tunnel problem while permitting wider MOSFET bus lines for improved drive. CMOS groups have just started to thin detectors for test. It will be interesting to see where this technology will lead in the future.

charge collection

The second operational task in generating an electronic image, charge collection, refers to the ability of the sensor to accurately reproduce an image after electrons are generated. Four parameters govern this process: the number of pixels on the chip, the number of signal charges a pixel can hold (also known as full well capacity), the variation in sensitivity from pixel to pixel, and the ability of a pixel to collect carriers efficiently without loss to its neighbors. CCDs hold the record for number of pixels, but CMOS engineers have designs with more than 4000 × 4000 pixels on the drawing board. Full well performance is comparable for the two technologies, although CCDs usually have a slight edge because the devices are driven with higher clock voltages that lead to greater well capacity. Pixel-to-pixel sensitivity nonuniformity, or fixed pattern noise (FPN), is primarily caused by slight size variations in the pixel's geometry defined at the fabrication foundry. Both technologies exhibit a nonuniformity of approximately 1% of the average signal level and therefore are comparable.

The fourth parameter, charge collection efficiency (CCE), is critical because it defines the spatial resolution of the detector. Ideally, the electrons generated due to photon exposure should remain in the target pixel. In the presence of a weak or nonexistent electric field, thermal diffusion can result in electrons wandering, or diffusing, into adjoining pixels, creating crosstalk. In the presence of an electric field, on the other hand, diffusion causes electrons to move but remain within the target pixel. Thermal diffusion makes the image appear out of focus and increases as pixel size shrinks (see figure 3 on page 32). Pixel crosstalk is most conspicuous for near-IR and soft x-ray photons that penetrate deep into the sensor, where very weak electric fields exist.

CCD manufacturers have eliminated

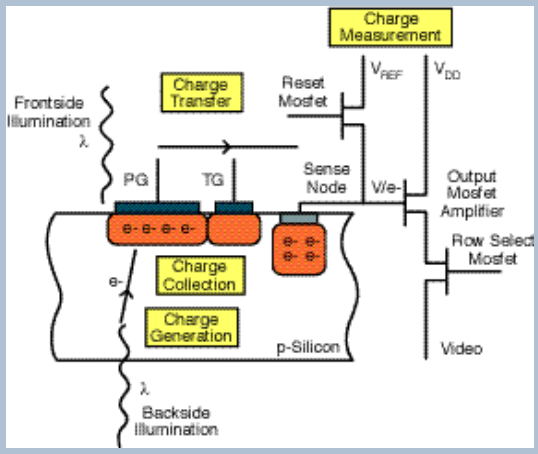

FIGURE 1 A cross-section of a CMOS pixel shows the four major functions required to generate an image.

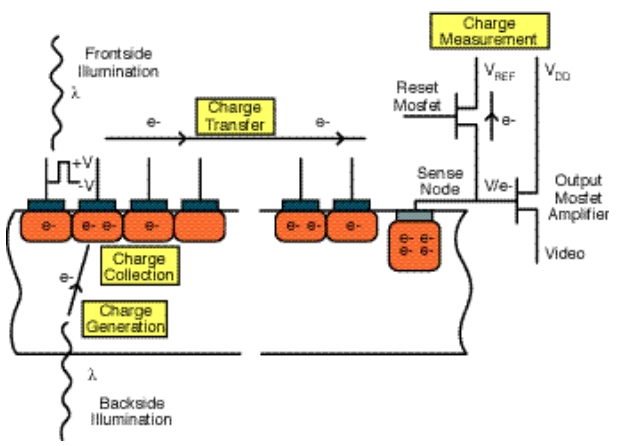

FIGURE 2 A cross-section of a CCD pixel shows the four major functions required to generate an image.

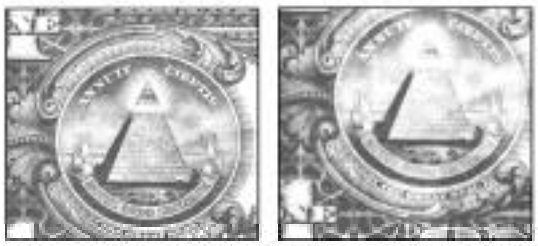

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FIGURE 3 4000 A and 9000 A images showing good and poor CCE performance because of charge diffusion, which is more prevalent as photons penetrate deeper into the array.

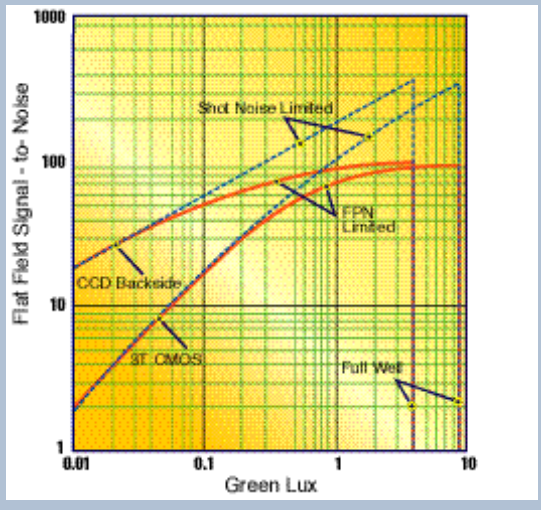

FIGURE 4 The flat field signal-to-noise performance as a function of green lux (4×10^{11} photons/cm^2-s) for a typical 3T CMOS array compared to a scientific backside-illuminated CCD array shows shot (dotted lines) and pixel nonuniformity (solid lines) noise-limited responses.

the negative effects of diffusion by using high-resistivity silicon wafers and high-voltage clocking to take advantage of the fact that the electric field depth varies as a function of the square root of resistivity and applied voltage. CCD electric fields typically extend 7 to 10 µm, allowing full spectral coverage into the near-IR spectral region (700 to 1100 nm).

In contrast, CCE performance for CMOS arrays has been relatively poor because standard foundry processes use low resistivity silicon and require low voltage drive. Typical electric field depths for CMOS processes extend only 1 to 2 µm, limiting spectral coverage to less than 650 nm. The silicon resistivity requirement is more critical for backside illuminated devices because thinning is limited to a dimension no thinner than approximately 8 µm. Therefore, high-resistivity material is required to generate collecting fields throughout the thinned membrane. The diffusion problem has forced CMOS groups to work with foundries that provide custom fabrication processes. Improvements in collection, however, may lead to other problems. For example, single-event upsets common to CMOS circuitry and ground bounce problems associated with on-chip logic circuitry become more pronounced as silicon resistivity increases.

charge transfer

The third operational task, charge transfer, is critically important to CCD operation. For very large arrays, a small charge packet may need to transfer through several inches in the silicon layer to reach the output amplifier. The signal channel must be void of electron traps induced by flaws in the design, processing, or even the silicon itself. For some scientific CCD applications, the charge transfer process must be 99.9999% efficient. This makes the CCD extremely sensitive to high-energy radiation sources that damage the silicon and induce electron traps—for example, high-energy protons in space.

In contrast, CMOS pixels are directly addressable and thus avoid many charge-transfer issues. However, high-performance CMOS pixels that transfer charge from a photo region to a readout region experience transfer problems. The ability of the sensor to completely transfer charge depends on the electric field strength between regions. Thus, requirements for low-voltage operation have made charge transfer challenging for CMOS groups, even though a single transfer is involved.

charge measurement

The last major operation is measuring the signal charge. The readout process for CMOS and CCD is identical. A capacitor connected to an output MOSFET amplifier converts signal charge to voltage. Designers have worked diligently to make this capacitor extremely small, which increases the gain of the amplifiers and gain of the output signal over noise sources. In addition, engineers design the geometry and electrical bias of the MOSFET to minimize noise from random fluctuations in the current flowing though the transistor. In theory, amplifiers in CMOS and CCD detectors should deliver the same noise level.

CCDs have pushed the read noise floor below 1 e- rms by running scans of less than 50 kpix/s (see figure 4). Low noise is achieved not just by careful amplifier design but also by the design of electronics that process the video signal. The raw output noise that accompanies a signal is between 20 and 100 e- rms, depending on the amplifier's sensitivity. Custom digital filtering circuits can reduce the noise level to theoretical levels. CCDs in the Hubble Space Telescope, for example, exhibit noise on the order of a few electrons.

CMOS detectors have considerably more difficulty achieving low-noise performance because analog process circuitry is on-chip. This requirement makes it tricky to optimally design low-noise circuits. For example, CCD cameras reject white noise by using capacitors to control the electrical bandwidth. CMOS designers do not have this luxury because adding filters would yield an excessively large chip. Hence, CMOS circuits usually work under open bandwidth conditions, which result in a noisier device.

Optimizing on-chip analog-to-digital converter (ADC) circuitry has also proven a challenge. Scientific CCDs often use 16-bit ADCs, which are very difficult to implement on CMOS arrays.

To achieve low-output amplifier noise, designers must contend with several other sources of noise. For example, the majority of CMOS pixels with their three-transistor readout are limited by so-called kTC reset noise, a large noise component that is generated when the sense-node capacitor is reset. The serial nature of CCD readout design allows reset noise to be completely removed by correlated double sampling circuits. For CMOS image sensors to compete, they require custom pixels that can read out charge transfer, similar to a CCD pixel. Thermal dark current and its associated noise also constitute an important difference between the two types of detectors. Manufacturers of CCDs have used custom processes, such as in multi-pinned-phase (MPP) CCDs, to reduce dark current to levels as low as 10 pA/cm^2 at 300 K.

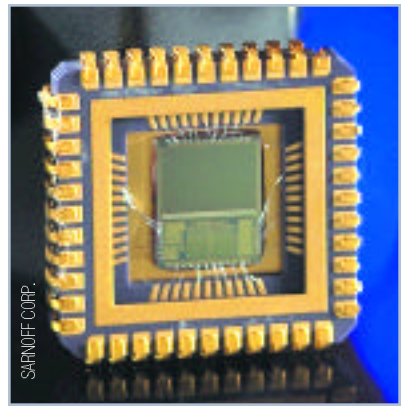

Figure 5 Pictured is a compact 640 × 480 CMOS video camera developed for low power operation.

Once again, CMOS sensors, which have dark currents from 100 to 2000 pA/cm^2, require custom designs and fabrication techniques to compete. CMOS sensors must also contend with numerous electrical ground-bounce noise problems generated by on-chip logic and ADC circuitry. These noise sources are very difficult to control in practice and quite often limit the sensor's noise floor above the reset noise level.

Even though CMOS designers currently face challenges in competing with scientific CCDs, the technology can be competitive in certain high-performance areas. CMOS readout has demonstrated significant advantages over CCDs for high-frame-rate scientific applications, for example. CMOS sensors typically read lines of pixels in a parallel fashion, usually with a signal processor circuit located in each column of the array. After critical analog sample-and-hold functions are completed, the processed data is then multiplexed into multiple channels to an ADC. Because CCDs are serial devices, single-channel processing results in a much higher pixel sample rate. For example, high-definition television CCDs read charge at better than 70 Mpixels/s, whereas the readout for CMOS HDTV arrays read at the line time (approximately 100,000 lines/s). Hence, CMOS read noise is considerably lower at high-frame rates.

CCDs and CMOS detectors clearly each have an advantage in particular areas. While engineers are making progress in improving the performance of the devices, it seems likely each technology will have its place in the imaging community. **oe**

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Reference:

1. Jim Janesick, Proc. SPIE vol. 4669A, paper #45, San Jose, CA (2002).

You can search for Janesick's book, *Scientific Charge-Coupled Devices*, on SPIE's bookstore (www.spie.org) to view the table of contents and preface.

watching the detectors

"It's curious how life works out," says James Janesick, director of the Sarnoff Corp. (Huntington Beach, CA) Advanced Sensors Group. "In 1972 my mom read a two-line advertisement in the *L.A. Times* stock-market section that said, 'Charge-coupled devices: JPL, an equal opportunity employer.'" Although doubtful that he would be hired, Janesick decided to answer the ad placed by the NASA government lab (Jet Propulsion Lab; Pasadena, CA). "I remember asking my boss-to-be, 'What's a CCD?'" says Janesick. "He said, "We don't know. But if you can find out, you've got the job."

So Janesick spent the next 22 years unraveling the mysteries and potential of the new sensor. He captured the first CCD image through his home telescope shortly after being hired. NASA subsequently equipped the Hubble Space Telescope, Galileo, and Cassini with camera systems developed by Janesick and his advanced development group. "The CCD was Hubble's showpiece and demonstrated the sensor's ultimate capability," says Janesick. He won two exceptional engineer medals from NASA for his research.

In 1995, when CCD development at JPL came to an end, Janesick opened a small company to develop high-speed CCDs for cinema photography applications. Eventually Janesick got curious about CMOS technology, so he transitioned to Conexant Systems Inc. (Newport Beach, CA). "Although it seemed sacrilegious to leave the CCD behind, I was curious about certain beliefs held by CMOS groups," he says—specifically, the rumor that said CCDs were going to become dinosaurs. "The CMOS projections were ahead of reality," he says. "The CCD is superior insofar as fundamental performance is concerned. For example, we could never fly CMOS imagers on applications like Hubble and likely never will." CMOS has many advantages over the CCD in the areas of chip integration and high-speed and low-cost applications, however. "The technologies will indeed coexist, and their niche will align to future applications invented," he says.

Janesick wrote a 900-page reference book titled *Scientific Charge-Coupled Devices*, published by SPIE in 2001, to celebrate the CCD's 30th birthday. In his spare time, Janesick plays guitar and piano. —*Laurie Ann Toupin*